

DATA SHEET

PEMD9; PUMD9
NPN/PNP resistor-equipped
transistors;
R1 = 10 k Ω , R2 = 47 k Ω

Product specification
Supersedes data of 2003 Nov 04

2004 Apr 15

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PEMD9; PUMD9

FEATURES

- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs.

APPLICATIONS

- Low current peripheral driver
- Replacement of general purpose transistors in digital applications
- Control of IC inputs.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V _{CEO}	collector-emitter voltage	–	50	V
I _O	output current (DC)	–	100	mA
TR1	NPN	–	–	–
TR2	PNP	–	–	–
R1	bias resistor	10	–	kΩ
R2	bias resistor	47	–	kΩ

DESCRIPTION

NPN/PNP resistor-equipped transistors in a SOT666 plastic package.

PRODUCT OVERVIEW

TYPE NUMBER	PACKAGE		MARKING CODE	PNP/PNP COMPLEMENT	NPN/PNP COMPLEMENT
	PHILIPS	EIAJ			
PEMD9	SOT666	–	D9	PEMB9	PEMH9
PUMD9	SOT363	SC-88	D*9 ⁽¹⁾	PUMB9	PUMH9

Note

- * = p: Made in Hong Kong.
 * = t: Made in Malaysia.
 * = W: Made in China.

SIMPLIFIED OUTLINE, SYMBOL AND PINNING

TYPE NUMBER	SIMPLIFIED OUTLINE AND SYMBOL	PINNING	
		PIN	DESCRIPTION
PEMD9; PUMD9	<p>Top view MAM448</p>	1	emitter TR1
		2	base TR1
		3	collector TR2
		4	emitter TR2
		5	base TR2
		6	collector TR1

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ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PEMD9	–	plastic surface mounted package; 6 leads	SOT666
PUMD9	–	plastic surface mounted package; 6 leads	SOT363

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per transistor; for the PNP transistor with negative polarity					
V_{CBO}	collector-base voltage	open emitter	–	50	V
V_{CEO}	collector-emitter voltage	open base	–	50	V
V_{EBO}	emitter-base voltage	open collector	–	10	V
V_I	input voltage TR1 positive negative		–	+40	V
			–	–6	V
V_I	input voltage TR2 positive negative		–	+6	V
			–	–40	V
I_o	output current (DC)		–	100	mA
I_{CM}	peak collector current		–	100	mA
P_{tot}	total power dissipation SOT363 SOT666	$T_{amb} \leq 25\text{ }^\circ\text{C}$;	–	–	
		note 1	–	200	mW
		notes 1 and 2	–	200	mW
T_{stg}	storage temperature		–65	+150	$^\circ\text{C}$
T_j	junction temperature		–	150	$^\circ\text{C}$
T_{amb}	operating ambient temperature		–65	+150	$^\circ\text{C}$
Per device					
P_{tot}	total power dissipation SOT363 SOT666	$T_{amb} \leq 25\text{ }^\circ\text{C}$;	–	–	
		note 1	–	300	mW
		notes 1 and 2	–	300	mW

Notes

1. Transistor mounted on an FR4 printed-circuit board, single-sided copper, standard footprint.
2. Reflow soldering is the only recommended soldering method.

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
Per transistor				
R _{th(j-a)}	thermal resistance from junction to ambient			
	SOT363	note 1	625	K/W
	SOT666	notes 1 and 2	625	K/W
Per device				
R _{th(j-a)}	thermal resistance from junction to ambient			
	SOT363	note 1	416	K/W
	SOT666	notes 1 and 2	416	K/W

Notes

1. Transistor mounted on an FR4 printed-circuit board, single-sided copper, standard footprint.
2. Reflow soldering is the only recommended soldering method.

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CHARACTERISTICS

$T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per transistor; for the PNP transistor with negative polarity						
I_{CBO}	collector-base cut-off current	$V_{\text{CB}} = 50\text{ V}$; $I_{\text{E}} = 0\text{ A}$	–	–	100	nA
I_{CEO}	collector-emitter cut-off current	$V_{\text{CE}} = 30\text{ V}$; $I_{\text{B}} = 0\text{ A}$	–	–	1	μA
		$V_{\text{CE}} = 30\text{ V}$; $I_{\text{B}} = 0\text{ A}$; $T_{\text{j}} = 150\text{ }^{\circ}\text{C}$	–	–	50	μA
I_{EBO}	emitter-base cut-off current	$V_{\text{EB}} = 5\text{ V}$; $I_{\text{C}} = 0\text{ A}$	–	–	150	μA
h_{FE}	DC current gain	$V_{\text{CE}} = 5\text{ V}$; $I_{\text{C}} = 5\text{ mA}$	100	–	–	
V_{CEsat}	collector-emitter saturation voltage	$I_{\text{C}} = 5\text{ mA}$; $I_{\text{B}} = 0.25\text{ mA}$	–	–	100	mV
$V_{\text{i(off)}}$	input-off voltage	$V_{\text{CE}} = 5\text{ V}$; $I_{\text{C}} = 100\text{ }\mu\text{A}$	–	0.7	0.5	V
$V_{\text{i(on)}}$	input-on voltage	$V_{\text{CE}} = 0.3\text{ V}$; $I_{\text{C}} = 1\text{ mA}$	1.4	0.8	–	V
$R1$	input resistor		7	10	13	$\text{k}\Omega$
$\frac{R2}{R1}$	resistor ratio		3.7	4.7	5.7	
C_{c}	collector capacitance					
	TR1 (NPN)	$V_{\text{CB}} = 10\text{ V}$; $I_{\text{E}} = i_{\text{e}} = 0\text{ A}$; $f = 1\text{ MHz}$	–	–	2.5	pF
	TR2 (PNP)		–	–	3	pF

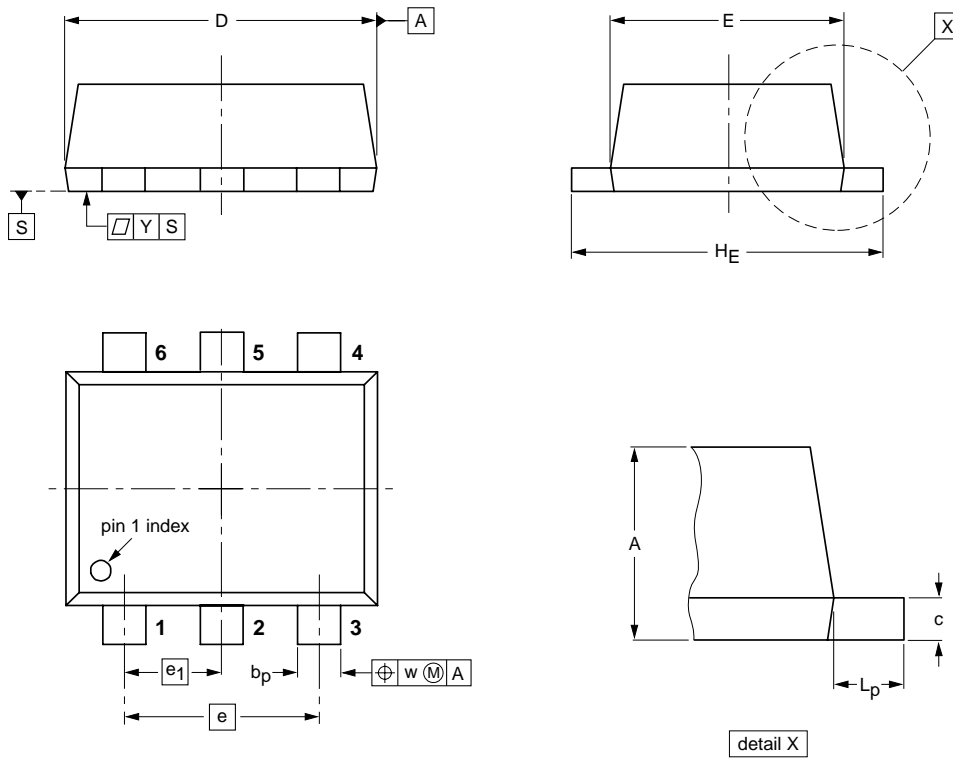
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PACKAGE OUTLINES

Plastic surface mounted package; 6 leads

SOT666



DIMENSIONS (mm are the original dimensions)

UNIT	A	b_p	c	D	E	e	e_1	H_E	L_p	w	y
mm	0.6 0.5	0.27 0.17	0.18 0.08	1.7 1.5	1.3 1.1	1.0	0.5	1.7 1.5	0.3 0.1	0.1	0.1

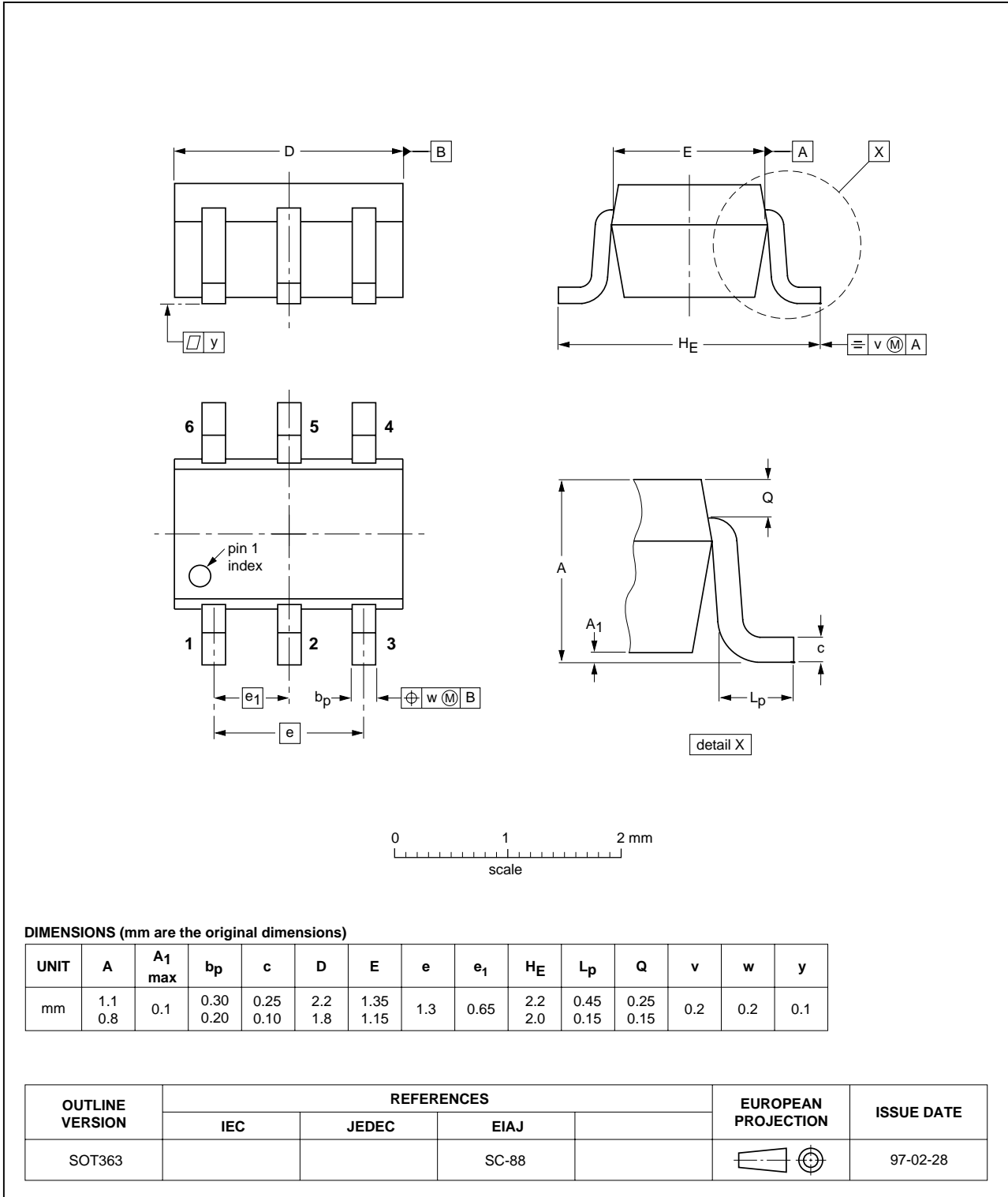
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT666					01-01-04 01-08-27

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DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
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3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Printed in The Netherlands

R75/05/pp9

Date of release: 2004 Apr 15

Document order number: 9397 750 13098

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